REMARKS/ARGUMENTS

Claims 1-44 are pending in this application, Claims 1, 22, 43 and 44 are amended. The Examiner has not acknowledged receipt of the IDS that was filed on October 16, 2000. Applicants respectfully request acknowledgment of the IDS by initialing and returning the attached copy of the same IDS.

Claims 1-9, 19-30 and 41-44 are rejected under 35 U.S.C. 103(a) as being obvious over Tseng et al. (U.S. Patent 6,009,256) in view of Schlansker et al. (U.S. Patent 6,408,428), and further in view of Kolchinsky et al. (U.S. Patent 5,535,406). Applicants submit that all of the pending claims are patentable over the cited references, and reconsideration and allowance of the pending claims are respectfully requested.

Amended independent claims 1, 22, 43 and 44 include, among other limitations, "a matrix describing different combinations of said plurality of hardware accelerators, said hardware dependent executable code, and variants to support run time execution of the plurality of kernel sections by the processing element array." Applicants respectfully submit that the cited references alone or in combination do not disclose or suggest the recited limitation.

Rather the system of Tseng "maps the selected hardware models into a reconfigurable hardware emulation board. In particular, step 307 takes "the netlist and maps the circuit design into specific FPGA chips." (Tseng et al., col. 19, lines 14-20). Tseng et al further teaches that "step 309 generates the configuration files for mapping the hardware model to FPGA chips. In essence, step 309 assigns circuit design components to

specific cells or gate level components in each chip." (Tseng et al., col. 19, lines 55-61).

Accordingly, there is no teaching or suggestion in Tseng of "a matrix describing different combinations of said plurality of hardware accelerators, said hardware dependent executable code, and variants."

Additionally, the specification of Tseng emphasizes: "In preparation for run-time, the software model in code form is stored in main memory where the application program associated with the SEmulation program in accordance with one embodiment of the present invention is stored. This code is processed in the general purpose processor or workstation 240. Substantially concurrently, the configuration file 220 for the hardware model is used to map the user circuit design into the reconfigurable hardware boards 250. Here, those portions of the circuit design that have been modeled in hardware are mapped and partitioned into the FPGA chips in the reconfigurable hardware boards 250." (Col. 16, lines 39-50). Additionally, the specification states "the user can perform emulation of the circuit design via software control," (col. 16, lines 54-55) and "[t]hus, the SEmulation system passes data between the test-bench 235 and the processor/workstation 240 for simulation and the test-bench 235 and the reconfigurable hardware boards 250 via data bus 245 and processor/workstation 240 for emulation. If a user target system 260 is involved, emulation data can pass between the reconfigurable hardware boards 250 and the target system 260 via the emulation interface 255 and data bus 245. The kernel is found in the software simulation model in the memory of the

processor/workstation 240 so data necessarily pass between the processor/workstation 240 and the reconfigurable hardware boards 250 via data bus 245. (Col. 16, line 62 to col. 17, line 6).

As a result, the system of Tseng does not generate code "to support run time execution of the plurality of kernel sections by the processing element array," as recited by the independent claims 1, 22, 43, and 44. Rather, the executable code of Tseng is run by the processor/workstation 240, not by the FPGA chips.

Furthermore, the system of Tseng dose not partition "the processing element array into a plurality of hardware accelerators," as recited by the independent claims 1, 43, and 44; neither does the system of Tseng include "a plurality of hardware accelerators partitioned from the processing element array," as recited by the independent claim 22. Rather, the system of Tseng maps and partitions those portions of the circuit design that have been modeled in hardware into the FPGA chips in the reconfigurable hardware boards 250. (Col. 16, lines 47-50). That is, the reconfigurable hardware boards of Tseng are not the equivalents of the processing element array of the present invention that are capable of executing the code.

Schlansker discloses a system for designing a VLIW processor using feedback about internal resource utilization by reading a specification of a candidate VLIW processor, which describes a specific instance of a parameterized processor design. The system then obtains internal resource usage statistics for the candidate processor. Similar to Tseng, Schlansker, alone or in combination with Tseng, does not teach

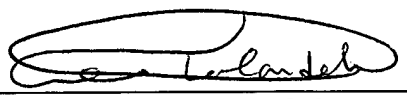
or suggest the above limitation required by the independent claims 1, 22, 43 and 44.

Kolchinsky describes a virtual processor with a reconfigurable, programmable logic array for processing data in accord with a hardware encoded algorithm. Likewise, Kolchinsky, alone or in combination with Tseng and/or Schlansker,does not teach or suggest the above limitation required by the independent claims 1, 22, 43 and 44.

Applicants therefore respectfully submit that independent claims 1, 22, 43 and 44 are novel and unobvious over the cited references and are therefore allowable. Applicants further submit that claims 2-21 and 23-42 that depend directly or indirectly from claims 1 and 22, respectively are allowable as are claims 1 and 22, and for additional limitations recited therein.

In view of the foregoing amendments and remarks, it is respectfully submitted that this application is now in condition for allowance, and accordingly, reconsideration and allowance are respectfully requested.

Respectfully submitted,
CHRISTIE, PARKER & HALE, LLP

By 

Raymond R. Tabandeh
Reg. No. 43,945
626/795-9900

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